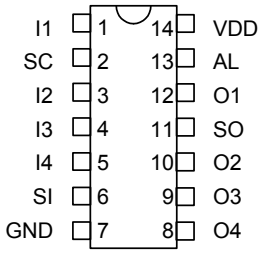
MONOLITHIC QUAD 4-BIT PROGRAMMABLE DELAY LINE (SERIES 3D7444)

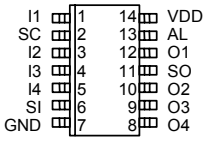
FEATURES

- Four indep't programmable lines on a single chip
- All-silicon CMOS technology
- Low quiescent current (1mA typical)
- Leading- and trailing-edge accuracy
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP pkg.)
- **Increment range:** 1.5ns through 25ns
- **Delay tolerance:** 1ns or 2% (See Table 1)
- **Temperature stability:** ±2% typical (0C-70C)
- **Vdd stability:** ±1% typical
- **Minimum input pulse width:** 10% of total delay

PACKAGES



DIP-14
3D7444-xx



SOIC-14
3D7444D-xx

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7444 device is a small, versatile, quad 4-bit programmable monolithic delay line. Delay values, programmed via the serial interface, can be independently varied over 15 equal steps. The step size (in ns) is determined by the device dash number. Each input is reproduced at the corresponding output without inversion, shifted in time as per user selection. For each line, the delay time is given by:

$$TD_n = T0 + A_n * TI$$

where T0 is the inherent delay, A_n is the delay address of the n-th line and TI is the delay increment (dash number). The desired addresses are shifted into the device via the SC and SI inputs, and the addresses are latched using the AL input. The serial interface can also be used to enable/disable each delay line. The 3D7444 operates at 5 volts and has a typical T0 of 6ns. The 3D7444 is CMOS-compatible, capable of sourcing or sinking 4mA loads, and features both rising- and falling-edge accuracy. The device is offered in a standard 14-pin auto-insertable DIP and a space saving surface mount 14-pin SOIC.

PIN DESCRIPTIONS

I1-I4	Signal Inputs
O1-O4	Signal Outputs
AL	Address Latch In
SC	Serial Clock In
SI	Serial Data In
SO	Serial Data Out
VDD	5.0V
GND	Ground

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DELAYS AND TOLERANCES (ns)			INPUT RESTRICTIONS			
	Delay Increment	Total Delay	Inherent Delay	Max Freq. (MHz)		Min P.W. (ns)	
				Recommended	Absolute	Recommended	Absolute
3D7444-1.5	1.5 ± 1.00	22.5 ± 1.0	6 ± 2.0	20.0	166	25.0	3.0
3D7444-2	2.0 ± 1.50	30.0 ± 1.0	6 ± 2.0	13.8	166	36.0	3.0
3D7444-4	4.0 ± 2.00	60.0 ± 1.2	6 ± 2.0	7.57	83.3	66.0	6.0
3D7444-5	5.0 ± 2.25	75.0 ± 1.5	6 ± 2.0	6.17	66.6	81.0	7.5
3D7444-8	8.0 ± 3.00	120 ± 2.4	6 ± 2.0	3.96	41.6	126.0	12.0
3D7444-10	10 ± 3.00	150 ± 3.0	6 ± 2.0	3.20	33.3	156.0	15.0
3D7444-15	15 ± 4.00	225 ± 4.5	6 ± 2.0	2.16	22.2	231.0	22.5
3D7444-20	20 ± 6.00	300 ± 6.0	6 ± 2.0	1.63	16.6	306.0	30.0
3D7444-25	25 ± 7.00	375 ± 7.5	6 ± 2.0	1.31	13.3	381.0	37.5

NOTES: Any increment between 1.5 and 25 ns not shown is also available as standard
Total delay is given by delay at address 15 minus delay at address 0

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APPLICATION NOTES

THEORY OF OPERATION

The quad 4-bit programmable 3D7444 delay line architecture is comprised of a number of delay cells connected in series with their respective outputs multiplexed onto the Delay Out pin (O1-O4) by the user-selected programming data. Each delay cell produces at its output a replica of the signal present at its input, shifted in time. Each of the four lines can be controlled independently, via the serial interface.

PROGRAMMED DELAY (ADDRESS) INTERFACE

Figure 1 illustrates the main functional blocks of the 3D7444 device. Since the device is a CMOS design, all unused input pins must be returned to well defined logic levels (VDD or GND). The delays are adjusted by first shifting a 20-bit programming word into the device via the SC and SI pins, then strobing the AL signal to latch the values. The bit sequence is shown in **Table 2**, and the associated timing diagram is shown in **Figure 2**. Each line has associated with it an enable bit. Setting this bit low will force the corresponding delay line output to a high impedance state, while setting it high returns the line to its normal operation. The device contains an SO output, which can be used to cascade multiple devices, as shown in Figure 3.

TABLE 2: BIT SEQUENCE

Bit	Delay Line	Function
1	4	Output Enable
2	3	Output Enable
3	2	Output Enable
4	1	Output Enable
5	1	Address Bit 3
6		Address Bit 2
7		Address Bit 1
8		Address Bit 0
9	2	Address Bit 3
10		Address Bit 2
11		Address Bit 1
12		Address Bit 0
13	3	Address Bit 3
14		Address Bit 2
15		Address Bit 1
16		Address Bit 0
17	4	Address Bit 3
18		Address Bit 2
19		Address Bit 1
20		Address Bit 0

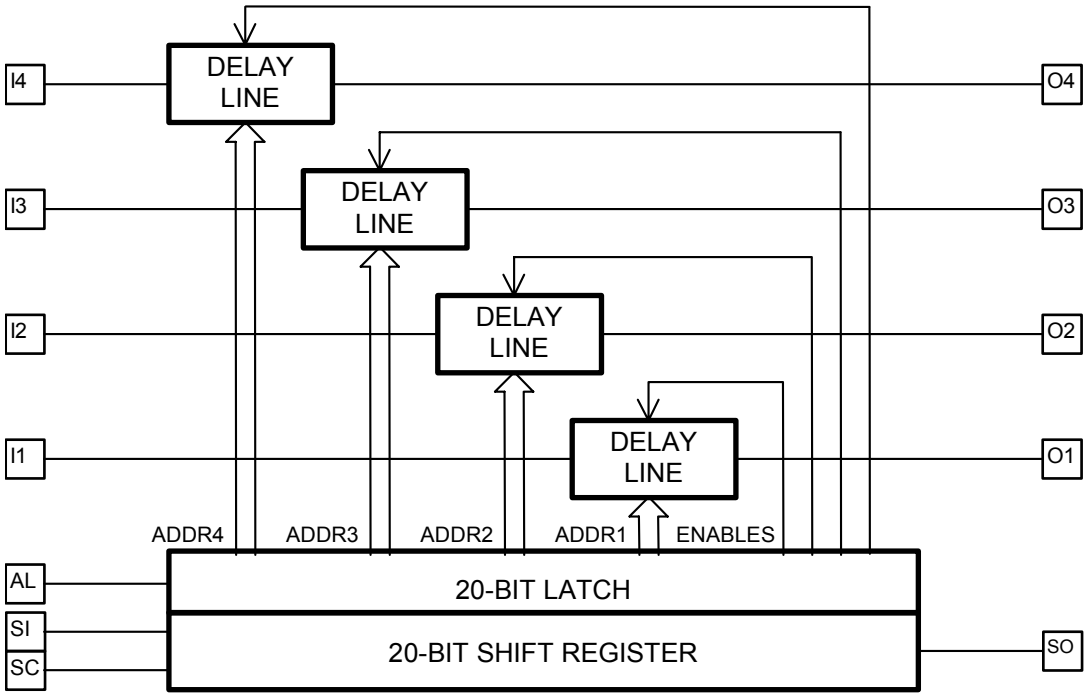


Figure 1: Functional block diagram

PROGRAMMED DELAY (ADDRESS) UPDATE

A delay line is a memory device. It stores information present at the input for a time equal to the delay setting before presenting it at the output with minimal distortion. Each 4-bit delay line in the 3D7444 can be represented by 15 serially connected delay elements (individually addressed by the programming data), each capable of storing data for a time equal to the device increment (step time). The delay line memory property, in conjunction with the operational requirement of "instantaneously" connecting the delay element addressed by the programming data to the output, may inject spurious information onto the output data stream. In order to ensure that spurious outputs do not occur, it is essential that the input signal be idle (held high or low) for a short duration prior to updating the programmed delay. This duration is given by the maximum programmable delay. Satisfying this requirement allows the delay line to "clear" itself of spurious edges. When the new address is loaded, the input signal can begin to switch (and the new delay will be valid) after a time given by $\mathbf{t_{PDV}}$ or $\mathbf{t_{EDV}}$ (see section below).

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D7444 programmable delay line utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The **thermal coefficient** is reduced to **400 PPM/C**, which is equivalent to a variation, over the 0C-70 C operating range, of **±2%** from the room-temperature delay settings. The **power supply coefficient** is reduced, over the 4.75V-5.25V operating range, to ±**1.5%** of the delay settings at the nominal 5VDC power supply and/or ±**2ns**, whichever is greater.

It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.

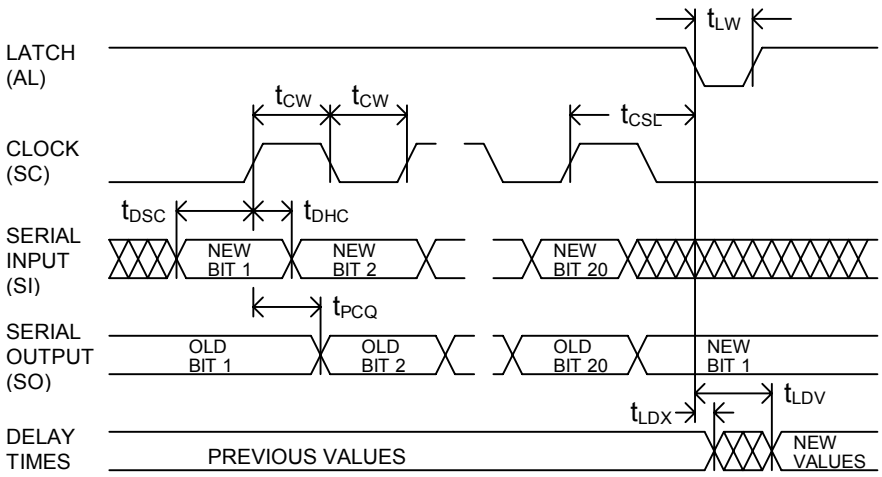


Figure 2: Serial interface timing diagram

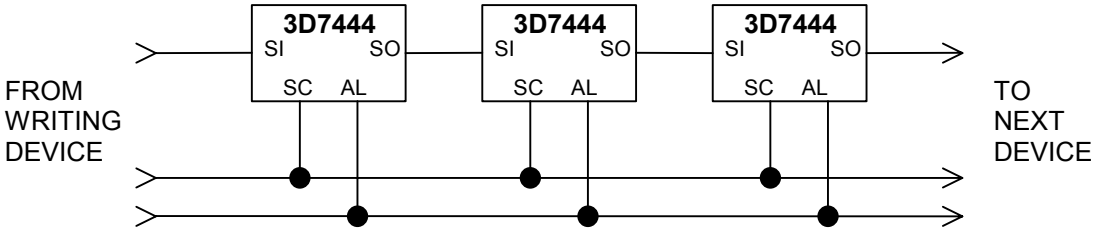


Figure 3: Cascading Multiple Devices

INPUT SIGNAL CONSIDERATIONS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay and increment accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a **Recommended** and an **Absolute Maximum** operating input frequency and a **Recommended** and an **Absolute Minimum** operating pulse width have been specified.

OPERATING FREQUENCY

The **Absolute Maximum Operating Frequency** specification, tabulated in **Table 1**, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The **Recommended Maximum Operating Frequency** specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed. Operation above the recommended maximum frequency will cause the delays to shift slighty with respect to their values at low-frequency operation. The magnitudes of these deviations will increase as the absolute maximum frequency is approached. However, if the input frequency and pulse width remain constant, the device will exhibit the same delays from one period to the next (ie, no appreciable jitter).

OPERATING PULSE WIDTH

The **Absolute Minimum Operating Pulse Width** (high or low) specification, tabulated in **Table 1**, determines the smallest pulse width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The **Minimum Operating Pulse Width** (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in **Table 1** is guaranteed.

Operation below the recommended minimum pulse width will cause the delays to shift slighty with respect to their values at long-pulse-width operation. The magnitudes of these deviations will increase as the absolute minimum pulse width is approached. However, if the input pulse width and frequency remain constant, the device will exhibit the same delays from one period to the next (ie, no appreciable jitter).

DEVICE SPECIFICATIONS

TABLE 3: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 4: DC ELECTRICAL CHARACTERISTICS

(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		1.3	2.0	mA	V_{DD} = 5.25V
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}	-0.1	0.0	0.1	µA	V_{IH} = V_{DD}
Low Level Input Current	I_{IL}	-0.1	0.0	0.1	µA	V_{IL} = 0V
High Level Output Current	I_{OH}		-8.0	-6.0	mA	V_{DD} = 4.75V V_{OH} = 2.4V
Low Level Output Current	I_{OL}	6.0	7.5		mA	V_{DD} = 4.75V V_{OL} = 0.4V
Output Rise & Fall Time	T_R & T_F		2		ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 4 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 5: AC ELECTRICAL CHARACTERISTICS

(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Latch Width	T_{LW}	10			ns	
Data Setup to Clock	t_{DSC}	10			ns	
Data Hold from Clock	t_{DHC}	1			ns	
Clock Width (High or Low)	t_{CW}	15			ns	
Clock Setup to Latch	t_{CSL}	20			ns	
Clock to Serial Output	t_{PCQ}		12	20	ns	
Latch to Delay Valid	t_{LDV}		35	45	ns	**1**
Latch to Delay Invalid	t_{LDX}	5			ns	**1**
Input Pulse Width	t_{WI}	10			% of Total Delay	See Table 1
Input Period	Period	20			% of Total Delay	See Table 1
Input to Output Delay	t_{PLH}, t_{PHL}				ns	See Text

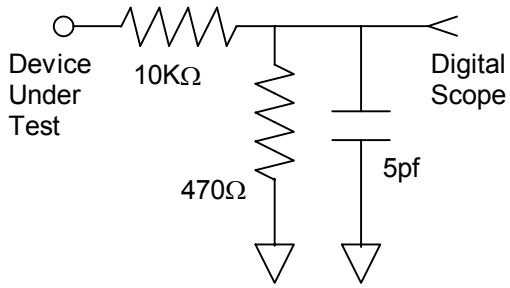
NOTES: 1 - Refer to **PROGRAMMED DELAY (ADDRESS) UPDATE** section

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (VDD): 5.0V ± 0.1V
Input Pulse: High = 3.3V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.7V)
Pulse Width: PW_{IN} = 1.25 x Total Delay
Period: PER_{IN} = 2.5 x Total Delay

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.65V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

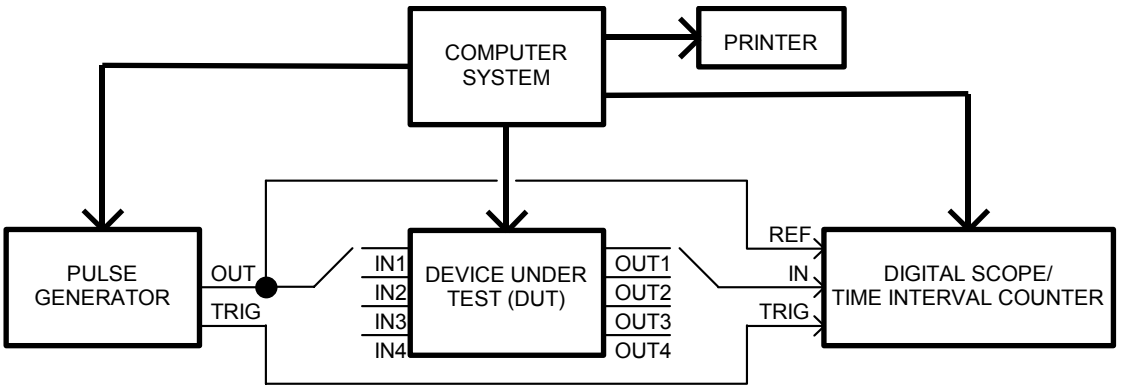


Figure 4: Test Setup

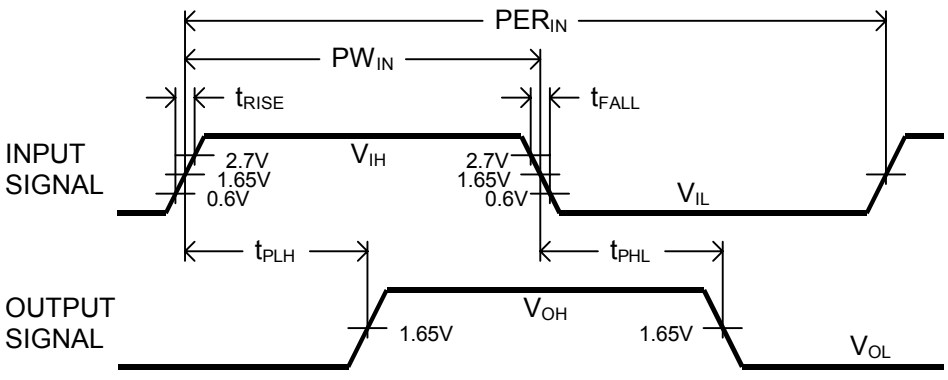


Figure 5: Timing Diagram